3652 Rec'd 10/06/03 #17

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Alexander Berger; Frank E. Kretz		
Assignee:	Tru-Si Technologies, Inc.		
Title:	Alignment of Semiconductor Wafers and Other Articles		
Application No.:	09/905,218	Filing Date:	July 13, 2001
Examiner:	Janice Lee Krizek	Group Art Unit:	3652
Docket No.:	M-11882 US		

San Jose, California
September 3, 2003

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(C) WITH FEE

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made, other than as described above; or

3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

Please charge the amount of $180.00 to Deposit Account No. 50-2257. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-2257. This paper is being submitted in duplicate.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 3, 2003.

Michael Shenker — 9-3-03
Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

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